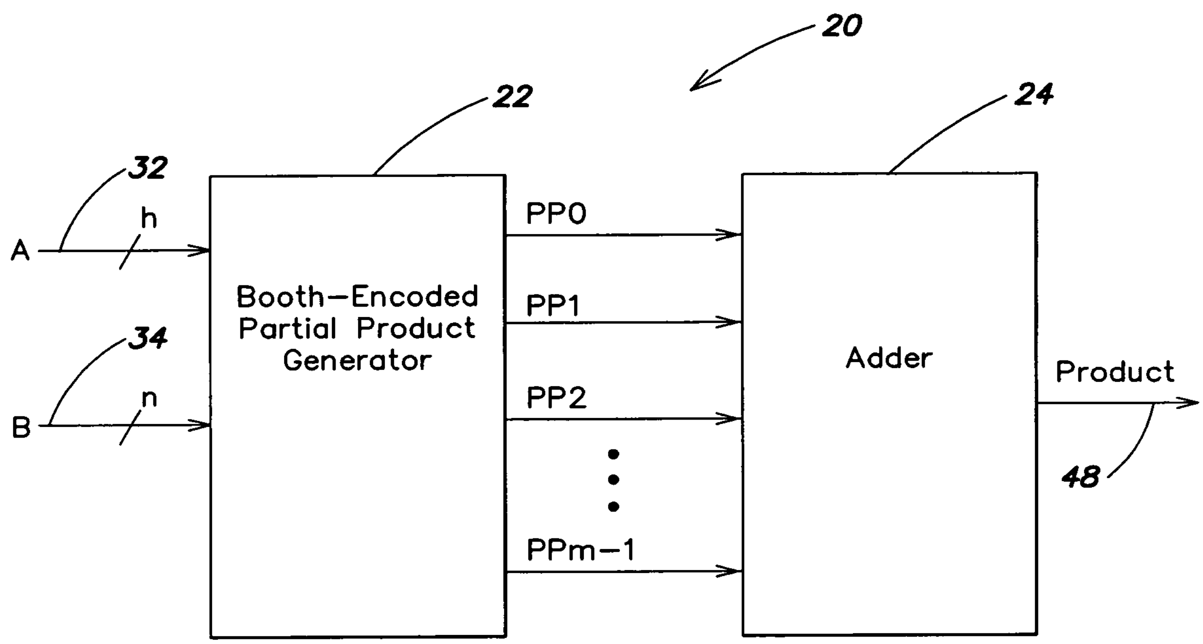

FIG. 1
(Prior Art)

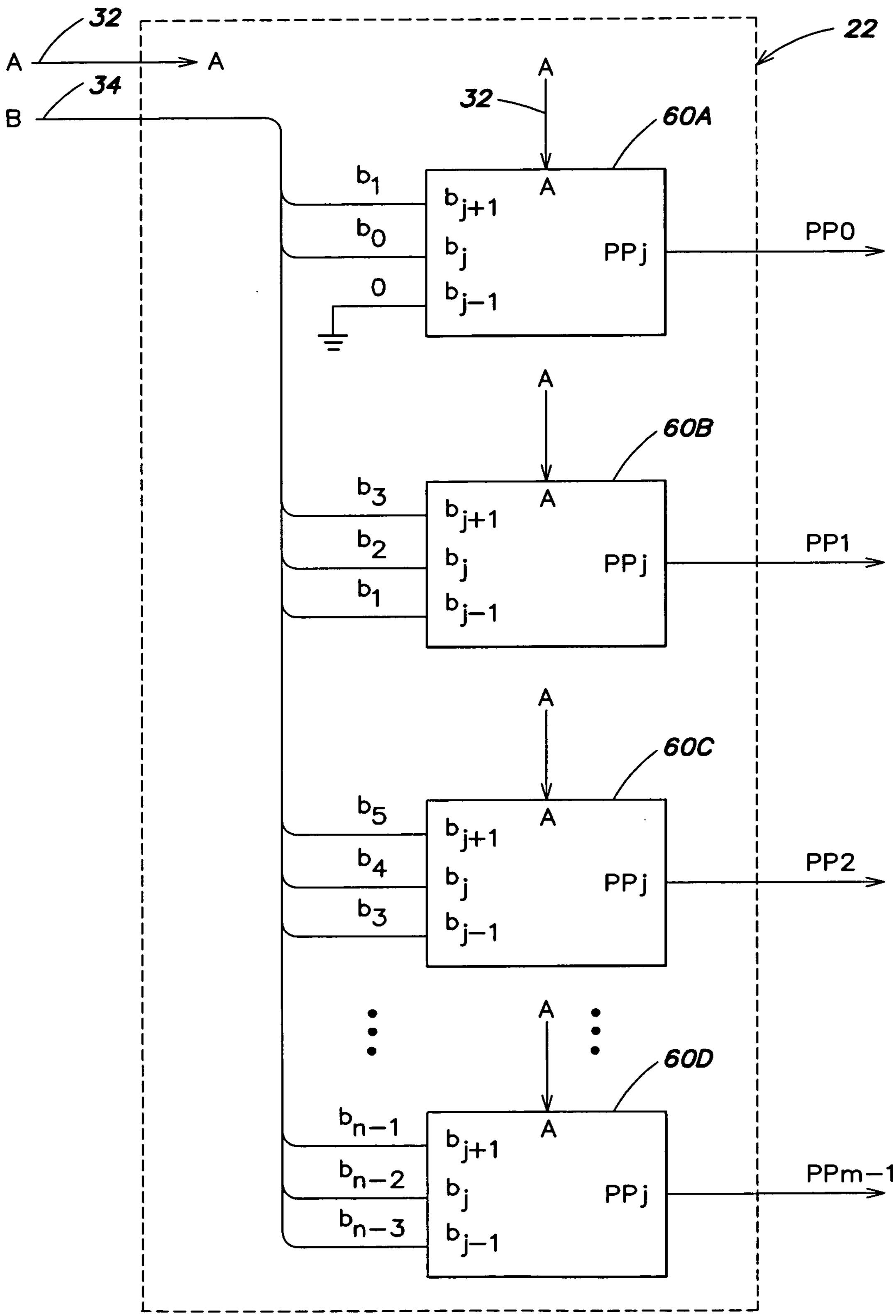

FIG. 2
(Prior Art)

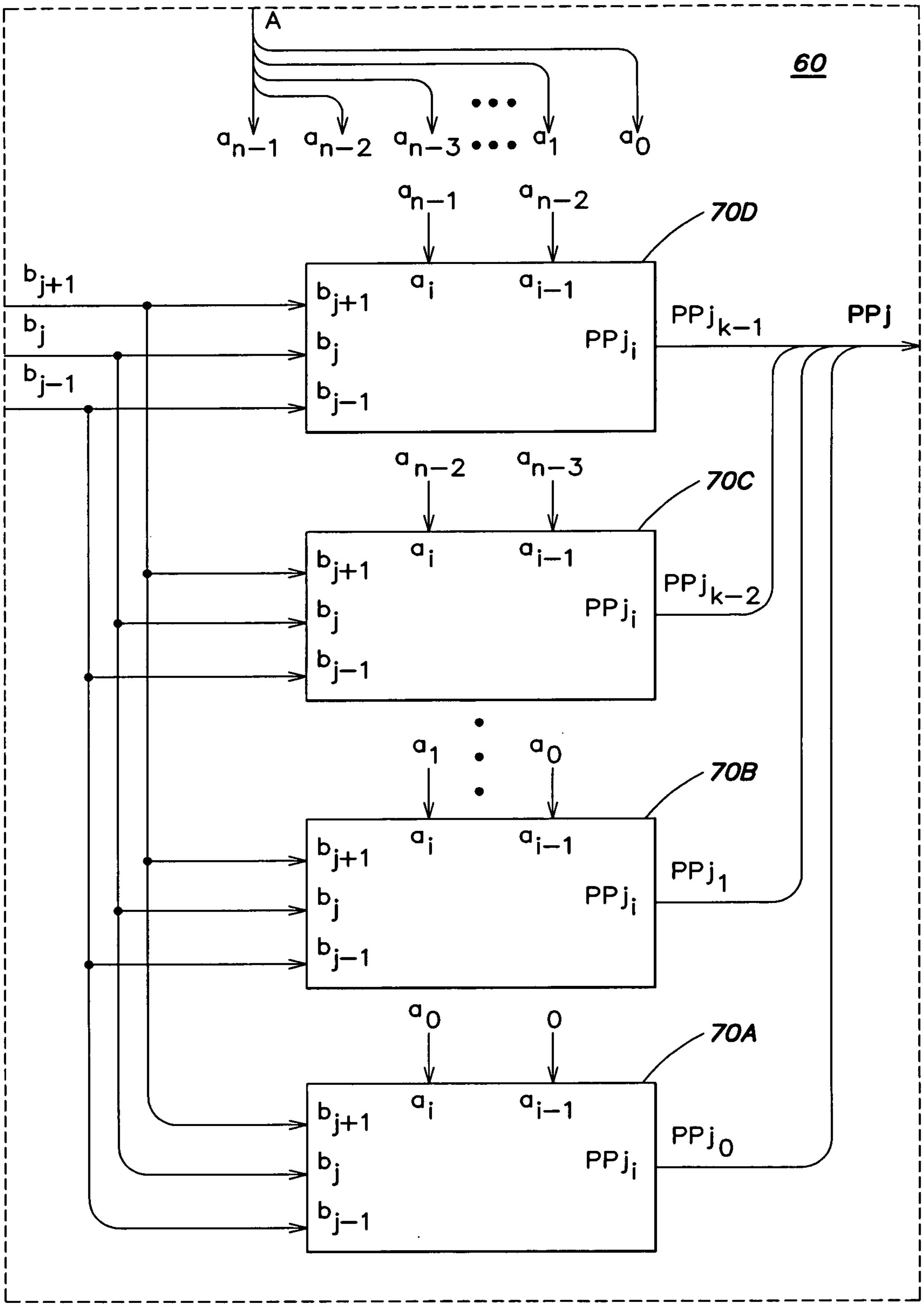

FIG. 3
(Prior Art)

$PPji = (a_i\ X_1 + a_{i-1}\ X_2) \oplus N$ eq. (1)

where

$X_1 = b_j \oplus b_{j-1}$ eq. (2)

$X_2 = \overline{b_{j+1}}\ b_j\ b_{j-1} + b_{j+1}\ \overline{b_j}\ \overline{b_{j-1}}$ eq. (3)

$N = b_{j+1}$ eq. (4)

FIG. 4A

(Prior Art)

b_{j+1}	b_j	b_{j-1}	X_1	X_2	N	PPj_i	PPj
0	0	0	0	0	0	0	0
0	0	1	1	0	0	a_i	A
0	1	0	1	0	0	a_i	A
0	1	1	0	1	0	a_{i-1}	2A
1	0	0	0	1	1	$\overline{a_{i-1}}$	−2A
1	0	1	1	0	1	$\overline{a_i}$	−A
1	1	0	1	0	1	$\overline{a_i}$	−A
1	1	1	0	0	1	0 * see note (1)	0 * see note (1)

Note (1)
In practice for the case of $bj{+}1\ bj\ bj{-}1$ = 1, 1, 1, the partial product bit PPj_i is frequently set equal to 1 in accordance with eq. (1) and therefore, the partial product PPj is equal to 1,...,1. However, the net effect of the partial product bit PPj_i and the partial product PPj to the adder 24 is 0 because a sign bit of 1 is added to the LSB of the partial product PPj during compressing in the adder.

FIG. 4B

(Prior Art)

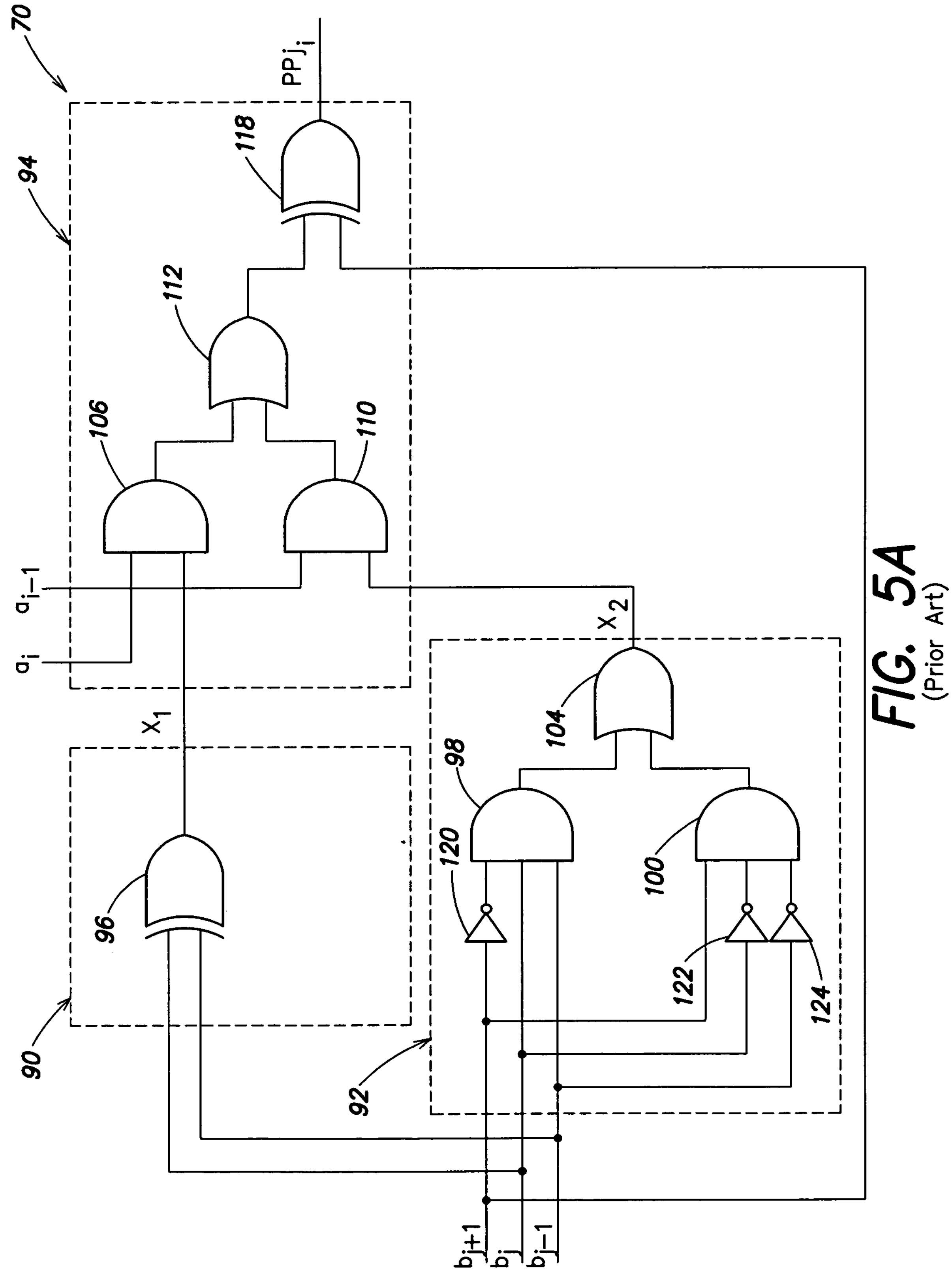

FIG. 5A
(Prior Art)

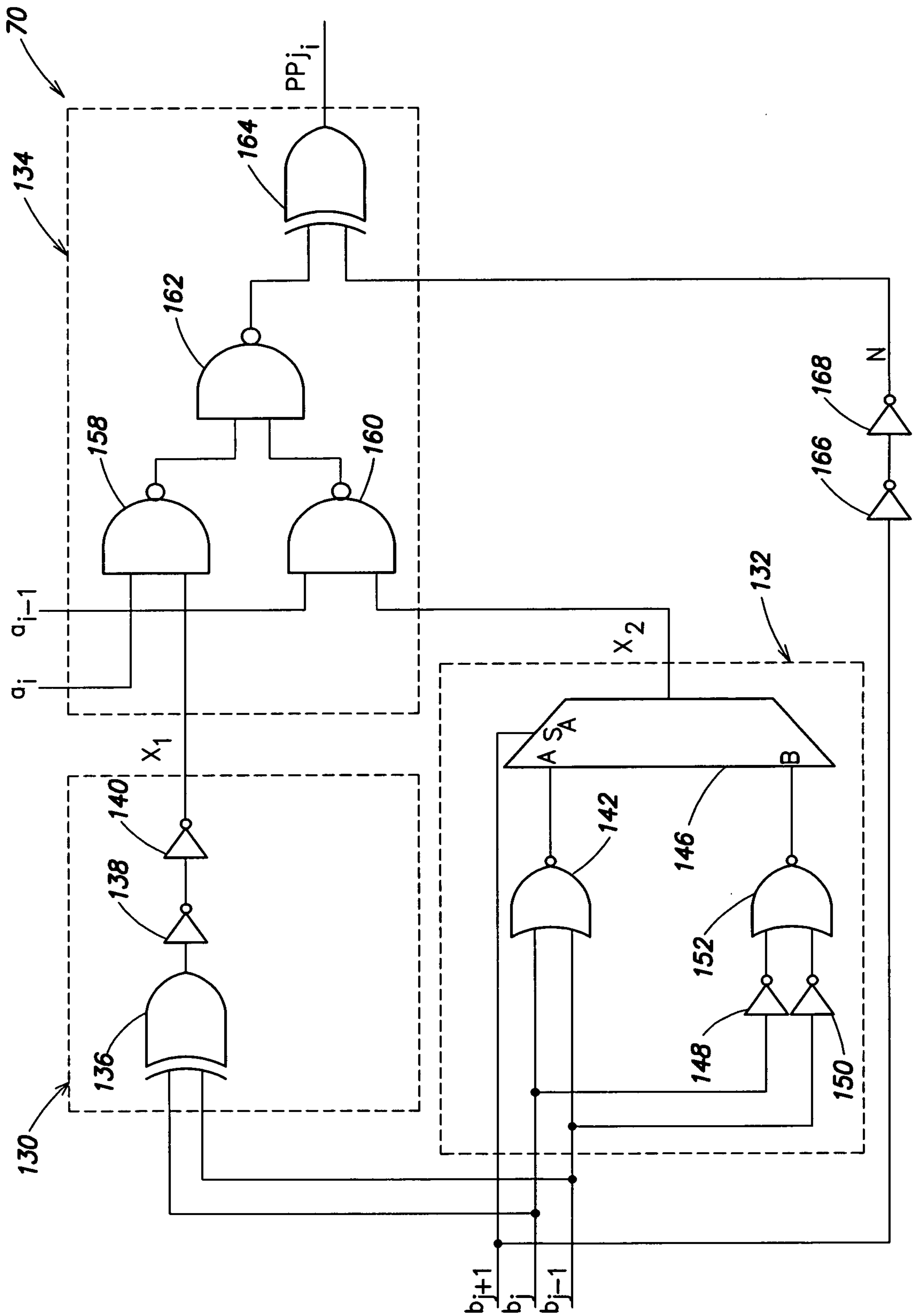

FIG. 5B
(Prior Art)

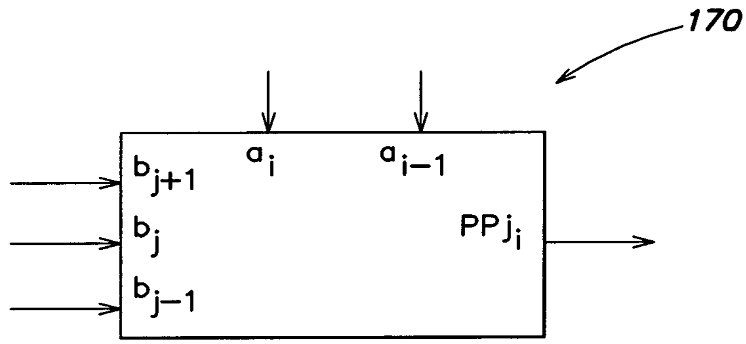

FIG. 6

$$PPj_i = s_{1,-1}\, aa_{1,-1} + s_2\, aa_2 + s_{-2}\, aa_{-2} \qquad \text{eqn. (5)}$$

where

$$s_{1,-1} = b_j \oplus b_{j-1} \qquad \text{eqn. (6)}$$

$$s_2 = b_j\ b_{j-1} \qquad \text{eqn. (7)}$$

$$s_{-2} = \overline{b_j}\ \overline{b_{j-1}} \qquad \text{eqn. (8)}$$

$$aa_{1,-1} = a_i \oplus b_{j+1} \qquad \text{eqn. (9)}$$

$$aa_2 = a_{i-1}\ \overline{b_{j+1}} \qquad \text{eqn. (10)}$$

$$aa_{-2} = \overline{a_{i-1}}\ b_{j+1} \qquad \text{eqn. (11)}$$

FIG. 7A

b_{j+1}	b_j	b_{j-1}	$s_{1,-1}$	s_2	s_{-2}	$aa_{1,-1}$	aa_2	aa_{-2}	PPj_i	PPj
0	0	0	0	0	1	a_i	a_{i-1}	0	0	0
0	0	1	1	0	0	a_i	a_{i-1}	0	a_i	A
0	1	0	1	0	0	a_i	a_{i-1}	0	a_i	A
0	1	1	0	1	0	a_i	a_{i-1}	0	a_{i-1}	2A
1	0	0	0	0	1	$\overline{a_i}$	0	$\overline{a_{i-1}}$	$\overline{a_{i-1}}$	−2A
1	0	1	1	0	0	$\overline{a_i}$	0	$\overline{a_{i-1}}$	$\overline{a_i}$	−A
1	1	0	1	0	0	$\overline{a_i}$	0	$\overline{a_{i-1}}$	$\overline{a_i}$	−A
1	1	1	0	1	0	$\overline{a_i}$	0	$\overline{a_{i-1}}$	0	0

FIG. 7B

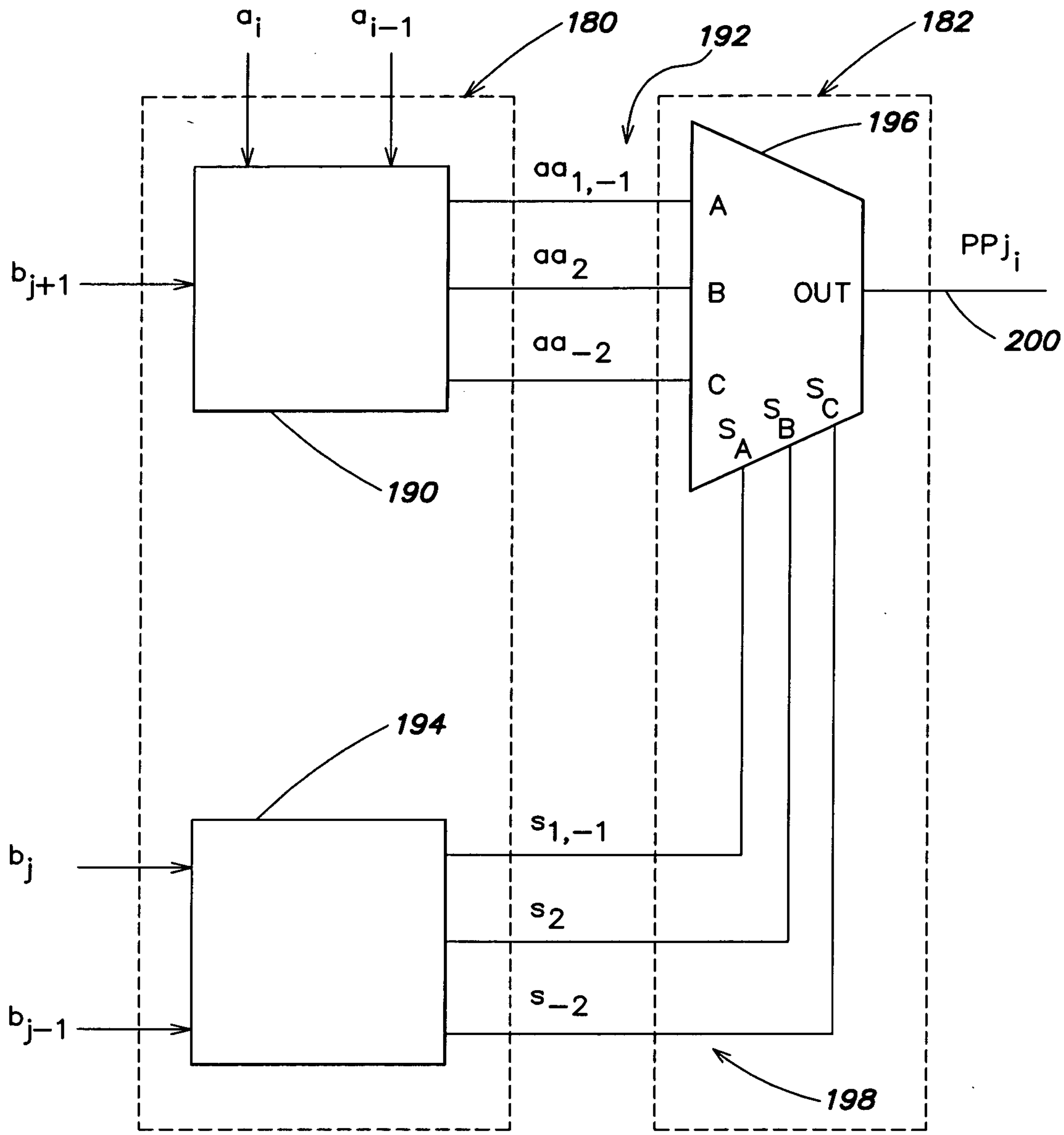
a_i
a_{i-1}
180
192
182
196
b_{j+1}
$aa_{1,-1}$
aa_2
aa_{-2}
A
B
C
OUT
PPj_i
200
S_A
S_B
S_C
190
194
b_j
b_{j-1}
$s_{1,-1}$
s_2
s_{-2}
198

FIG. 8

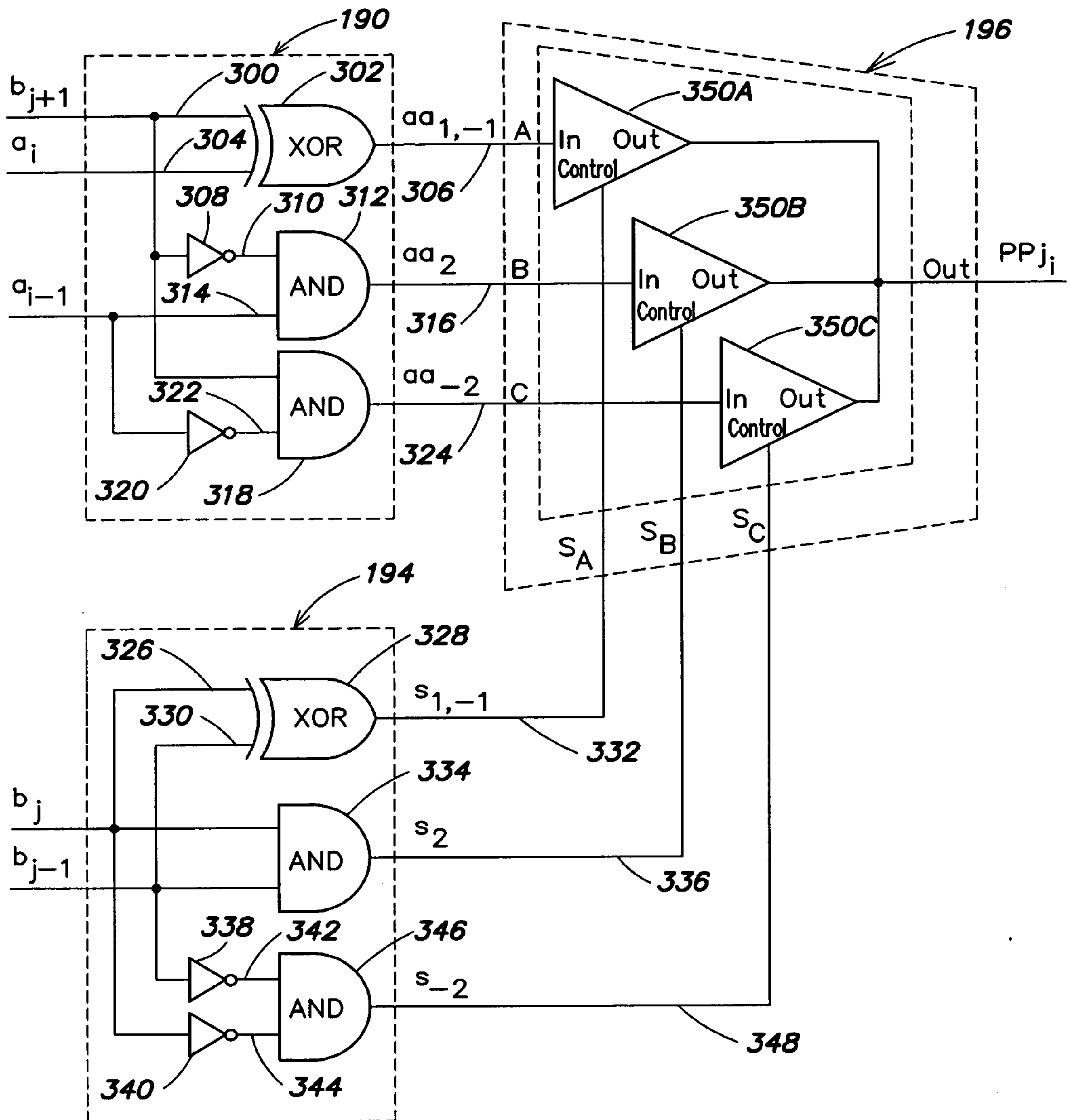
190
196
300
302
304
b_{j+1}
a_i
XOR
$aa_{1,-1}$
A
306
350A
In Out
Control
308
310
312
350B
a_{i-1}
AND
aa_2
B
314
316
Out
PPj_i
350C
AND
aa_{-2}
C
322
324
320
318
S_A
S_B
S_C
194
326
328
330
XOR
$s_{1,-1}$
332
334
b_j
b_{j-1}
AND
s_2
336
338
342
346
AND
s_{-2}
340
344
348

FIG. 9

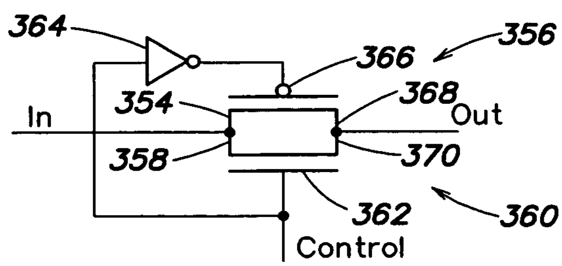
364
356
366
354
368
Out
In
358
370
362
360
Control

FIG. 10

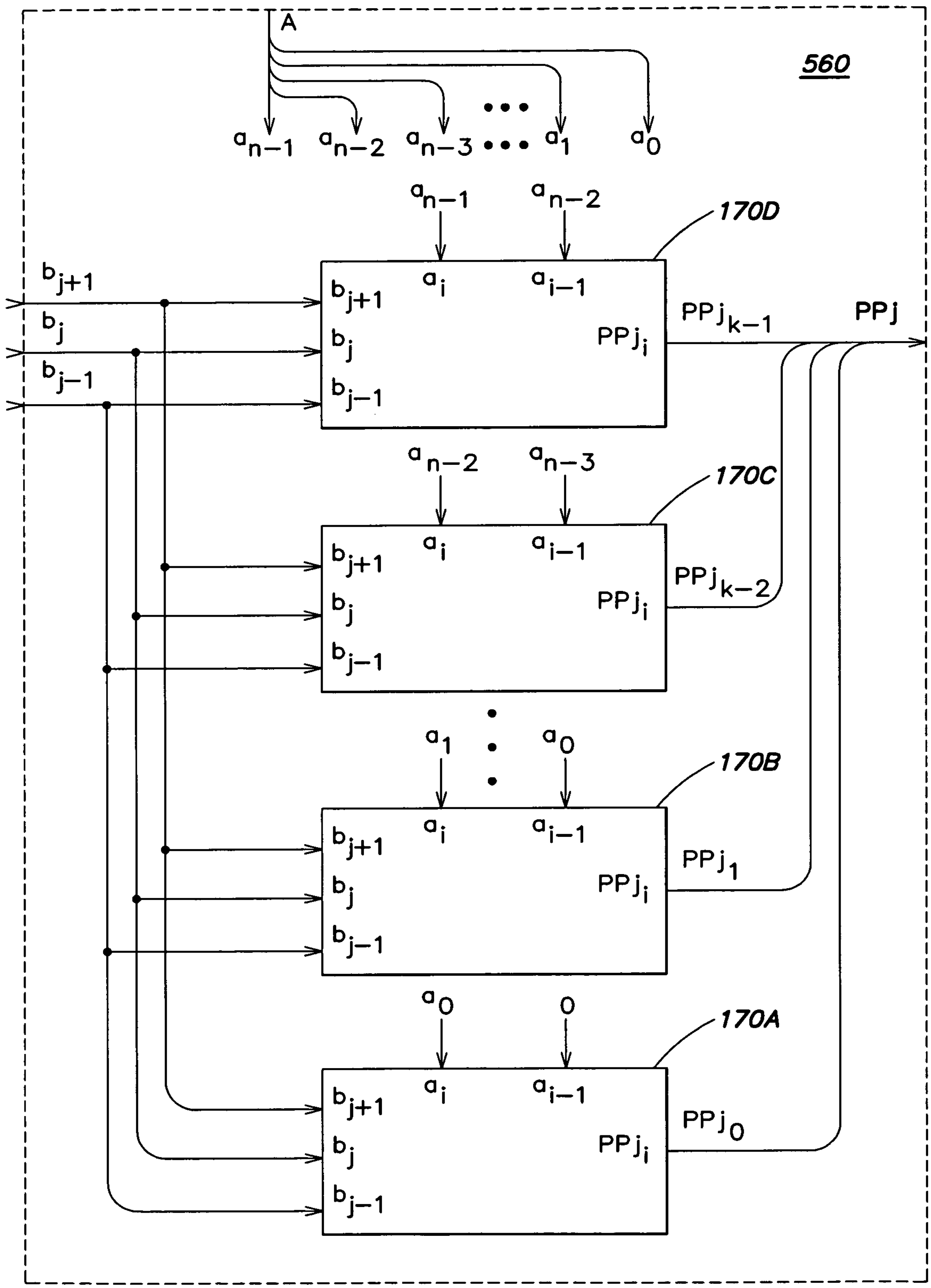
A
560
a_{n-1} a_{n-2} a_{n-3} ••• a_1 a_0
a_{n-1} a_{n-2}
170D
b_{j+1}
b_j
b_{j-1}
a_i a_{i-1}
PPj_i
PPj_{k-1}
PPj
a_{n-2} a_{n-3}
170C
PPj_{k-2}
a_1 a_0
170B
PPj_1
a_0 0
170A
PPj_0

FIG. 11

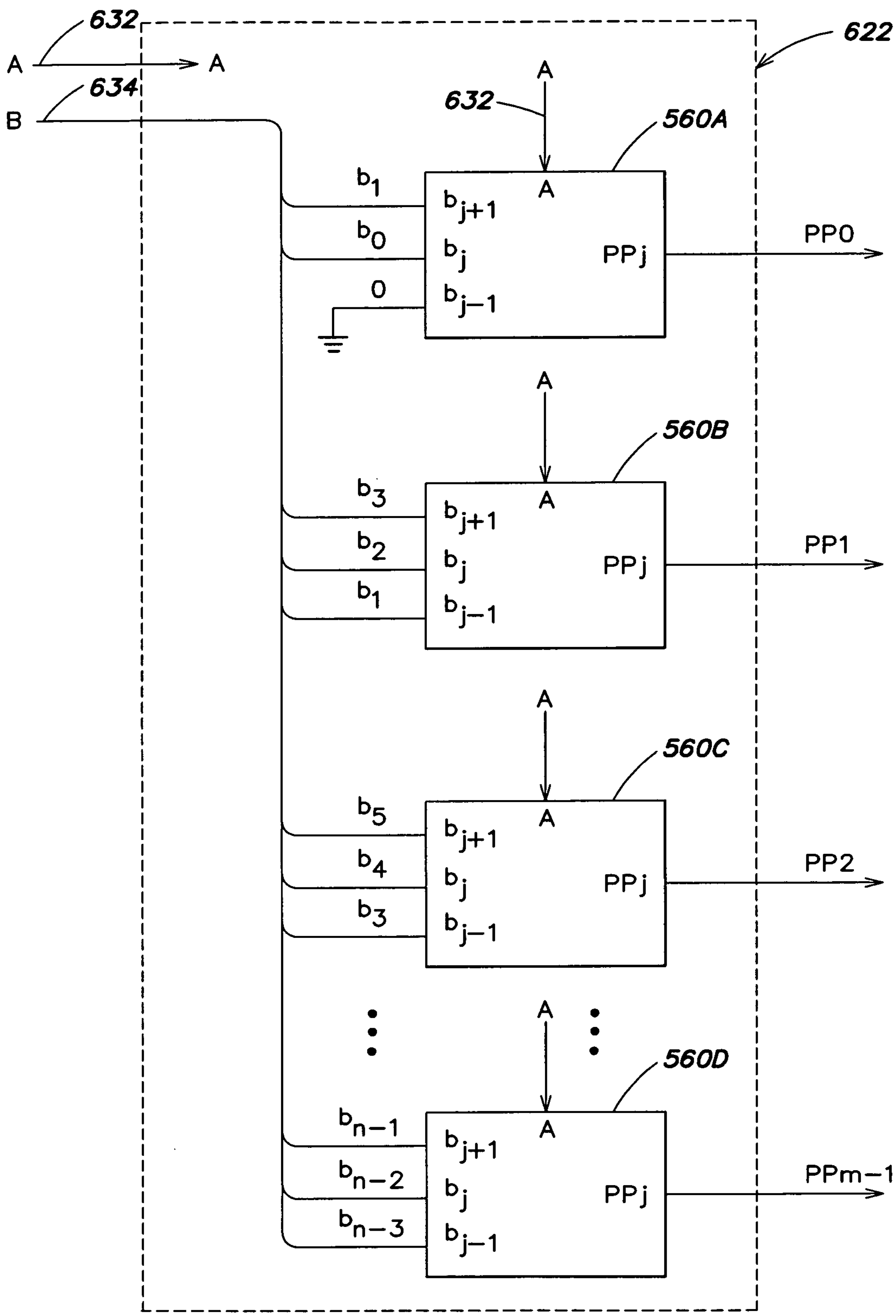
632
A
A
634
B
622
A
632
560A
b_1
A
b_{j+1}
b_0
b_j
PPj
PP0
0
b_{j-1}
A
560B
b_3
A
b_{j+1}
b_2
b_j
PPj
PP1
b_1
b_{j-1}
A
560C
b_5
A
b_{j+1}
b_4
b_j
PPj
PP2
b_3
b_{j-1}
A
560D
b_{n-1}
A
b_{j+1}
b_{n-2}
b_j
PPj
PPm−1
b_{n-3}
b_{j-1}

FIG. 12

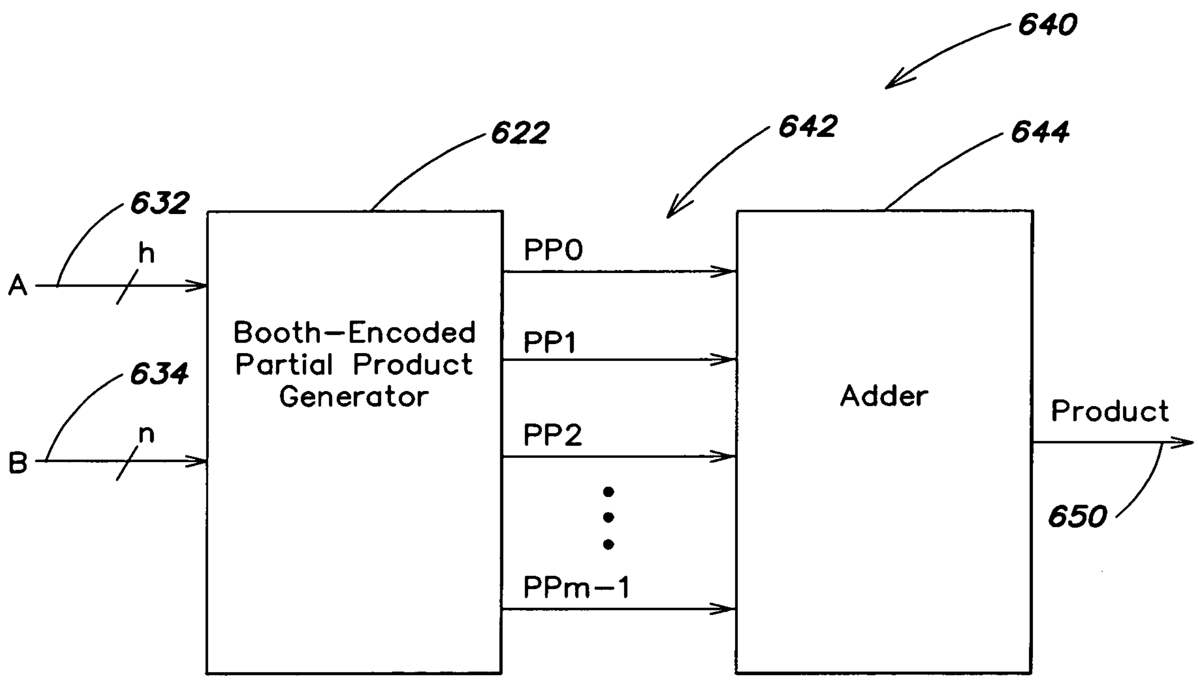
640
622
642
644
632
634
A
h
B
n
Booth–Encoded Partial Product Generator
PP0
PP1
PP2
PPm–1
Adder
Product
650

FIG. 13